



MS-7642 VER:10

CPU:

AMD AM3 (HT 3.0)

System Chipset:

AMD/ATI RS880D

AMD/ATI SB850

On Board Chipset:

FINTEK Super I/O -- F71889

LAN -- RTL8111DL

HD Codec -- ALC889

USB3.0 -- NEC uPD720200

PATA -- JMICRON JMB368

BIOS -- SPI ROM 8M

Main Memory:

DDR III X 4 (Max 8GB)

Expansion Slots:

PCI-E X 16 *2

PCI-E X 1 *1

PCI 2.2 Slot X 1

Clock Generator:

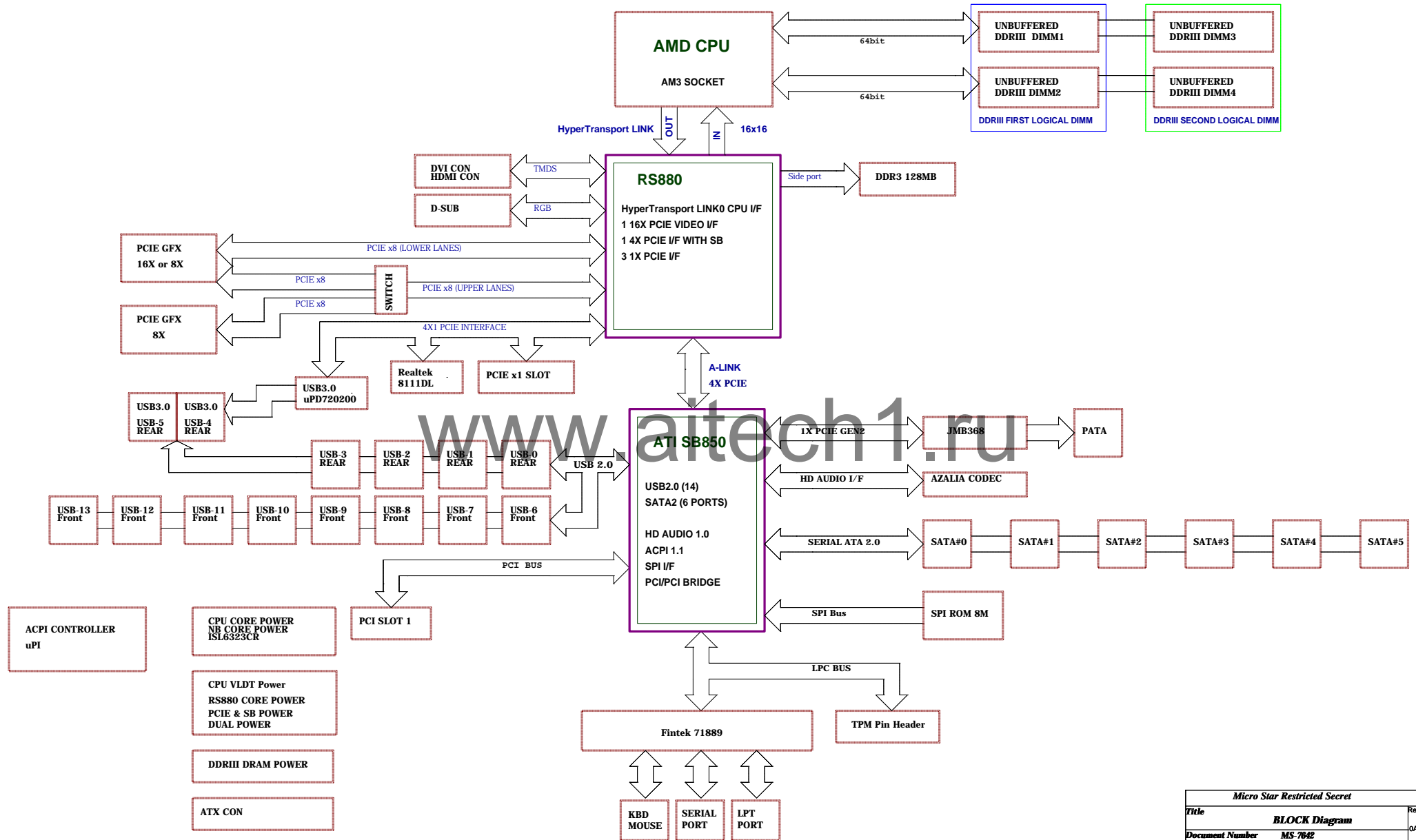
Controller--REALTEK RTM880N-793

PWM:

ISL6323+ISL6212

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Project RS-880D BLOCK DIAGRAM

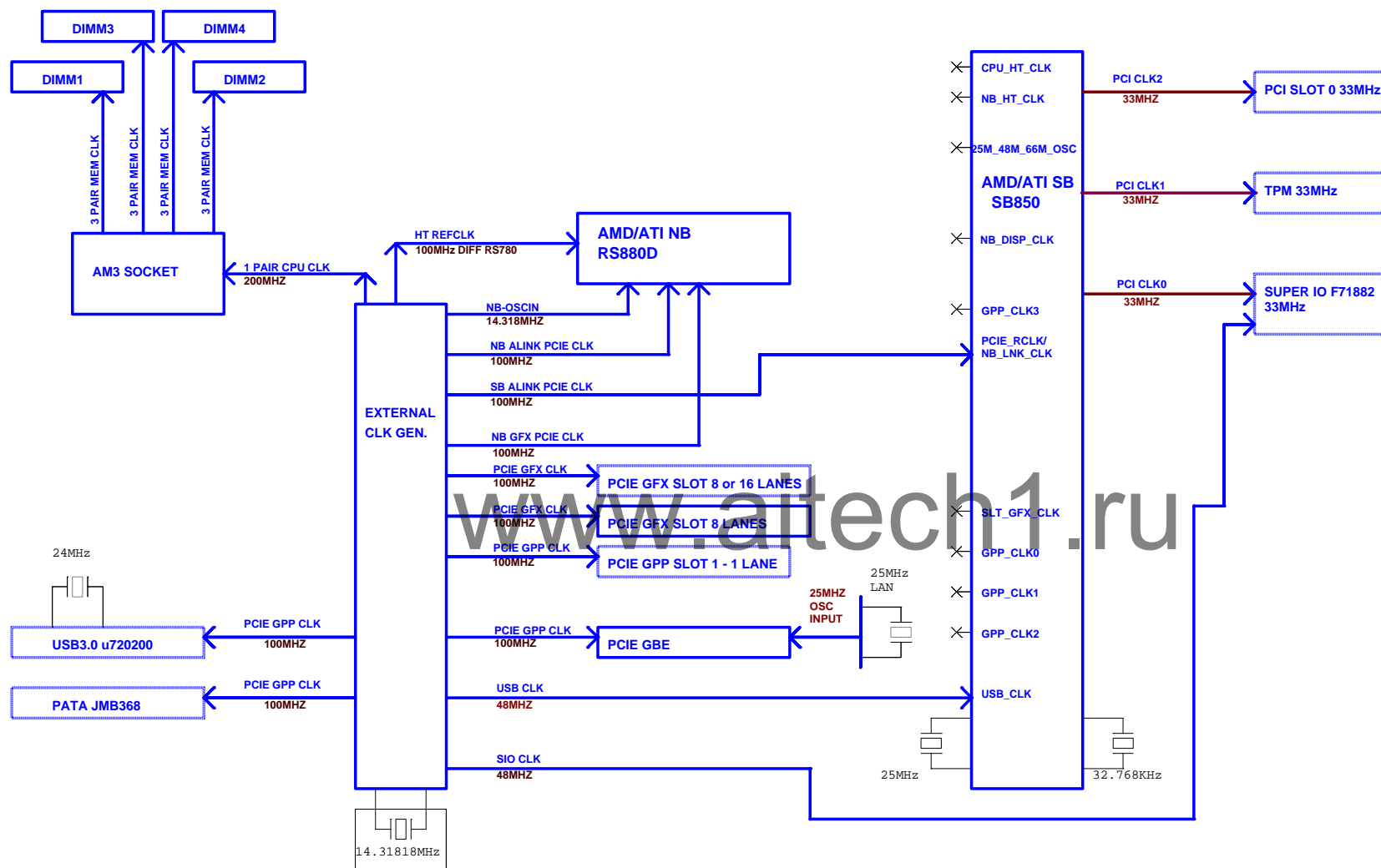


F71889 GPIO Config

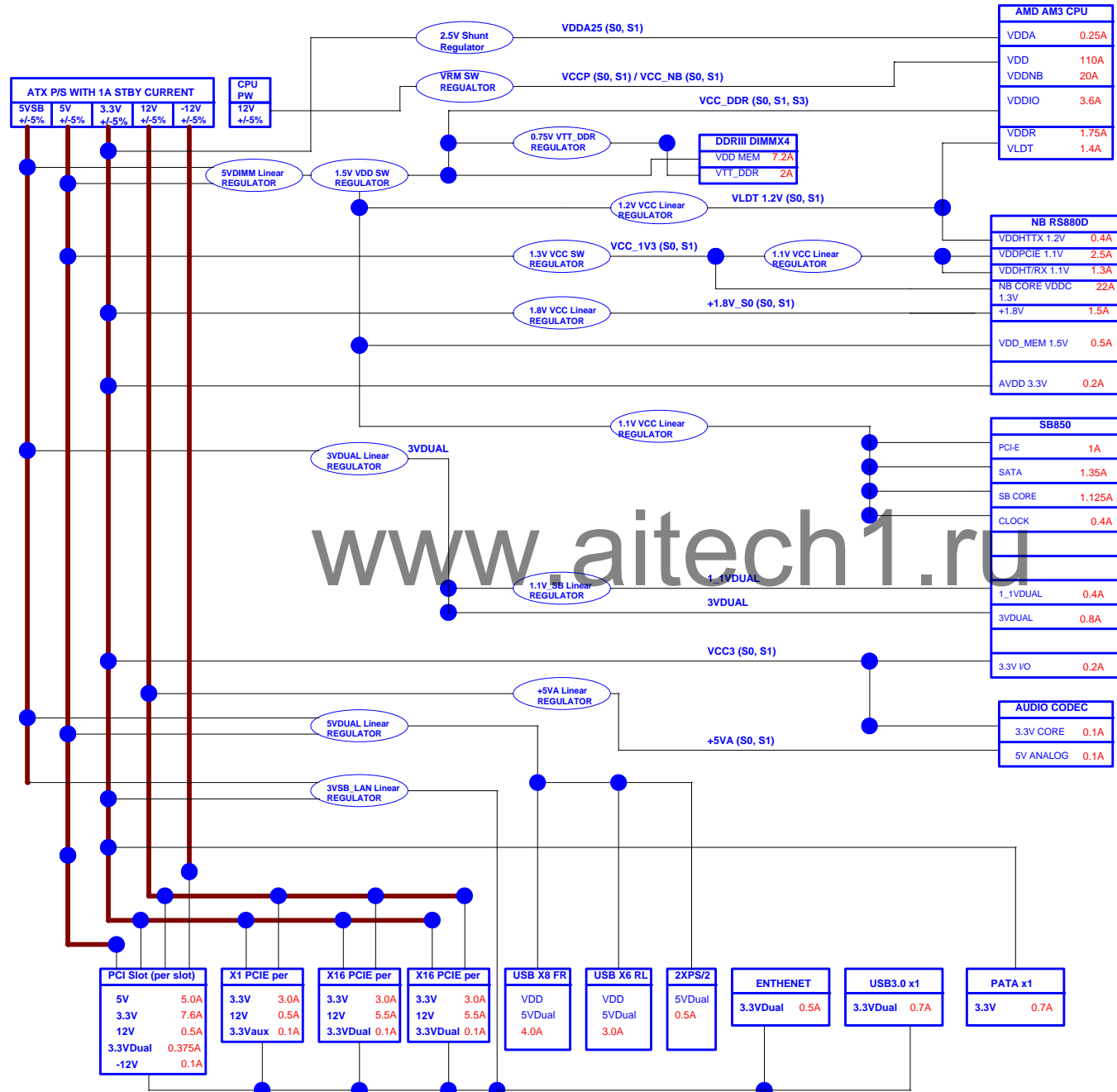
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www.aitech1.ru

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD21	PCICLK0



Power Deliver Chart



AMD AM3 CPU	
VDDA	0.25A
VDD	110A
VDDNB	20A
VDDIO	3.6A
VDDR	1.75A
VLDT	1.4A

NB RS880D	
VDDHTTX 1.2V	0.4A
VDDPCIE 1.1V	2.5A
VDDHT/RX 1.1V	1.3A
NB CORE VDDC 1.3V	22A
+1.8V	1.5A
VDD_MEM 1.5V	0.5A
AVDD 3.3V	0.2A

SB850	
PCI-E	1A
SATA	1.35A
SB CORE	1.125A
CLOCK	0.4A
1_1VDUAL	0.4A
3VDUAL	0.8A
3.3V I/O	0.2A

AUDIO CODEC	
3.3V CORE	0.1A
5V ANALOG	0.1A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3VDual	0.375A
-12V	0.1A

X1 PCIe per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIe per	
3.3V	3.0A
12V	5.5A
3.3VDual	0.1A

X16 PCIe per	
3.3V	3.0A
12V	5.5A
3.3VDual	0.1A

USB X8 FR
VDD
5VDual
4.0A

USB X6 RL	2
VDD	5
5VDual	0
3.0A	

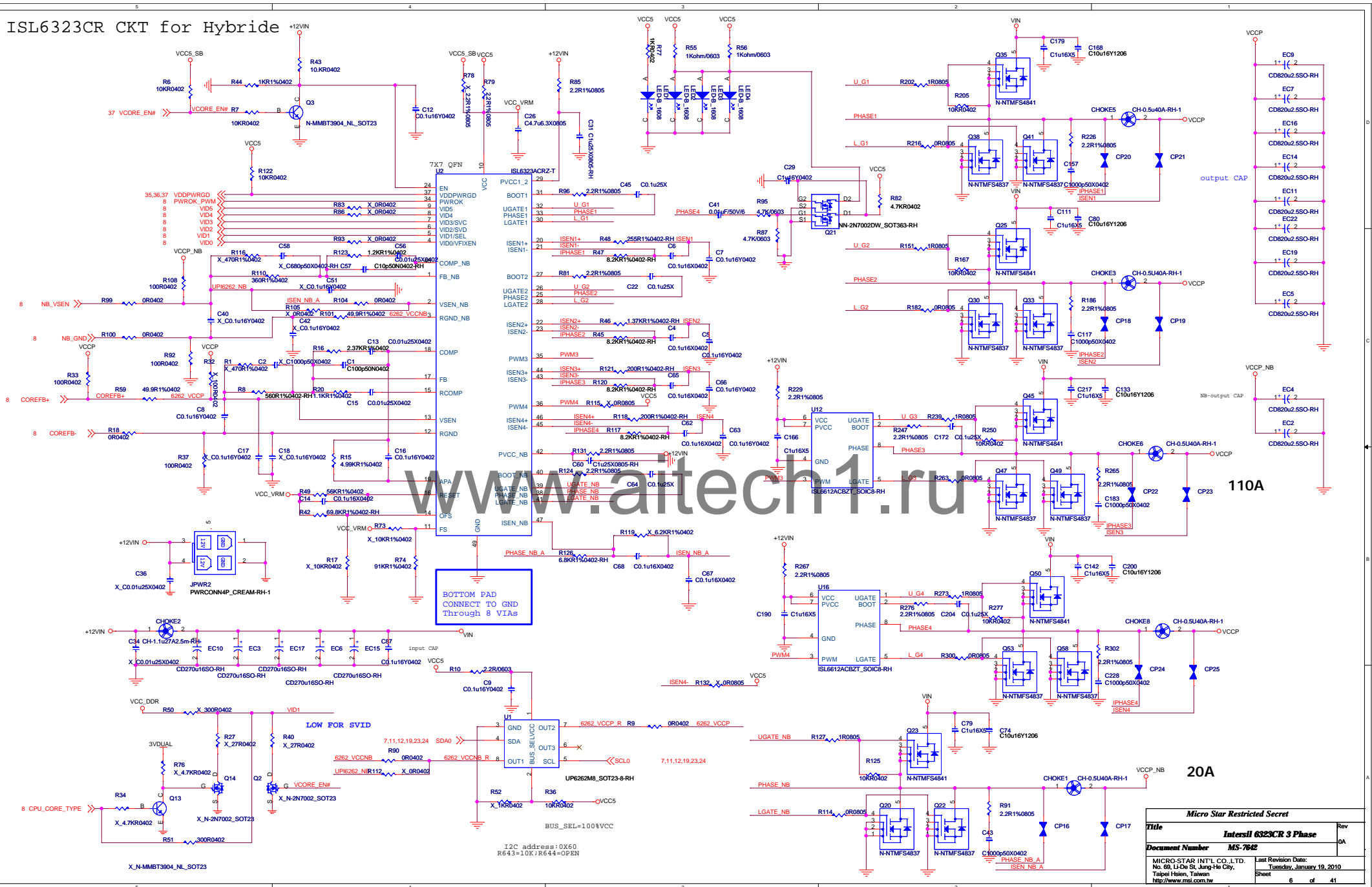
PS/2	ENT
Dual	3.3V Du
5A	

HENET	
0.5A	3.3

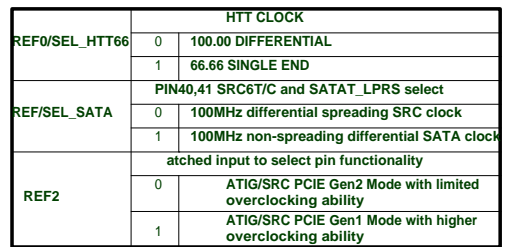
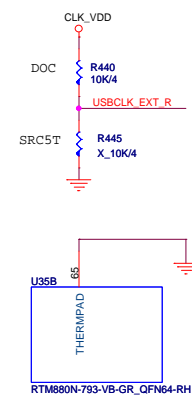
USB3.0 x1
7Dual 0.7A

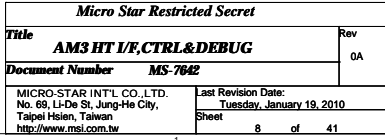
PATA x1
3.3V 0.7A

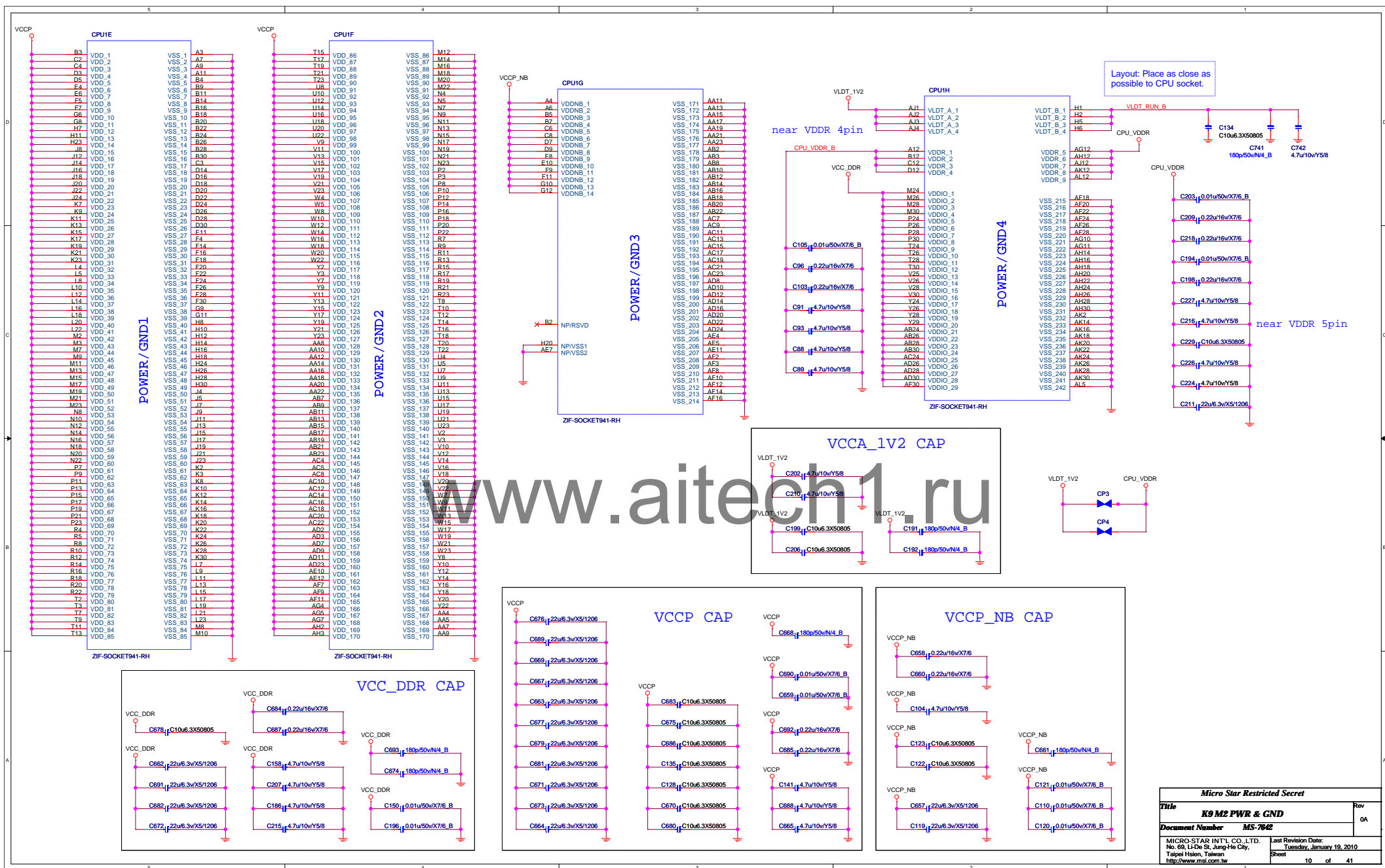
ISL6323CR CKT for Hybride

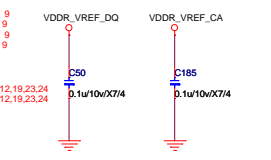
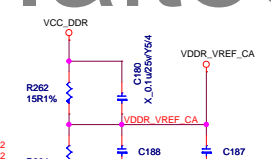
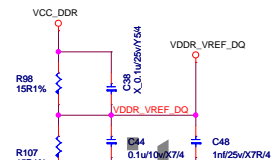
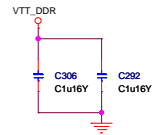


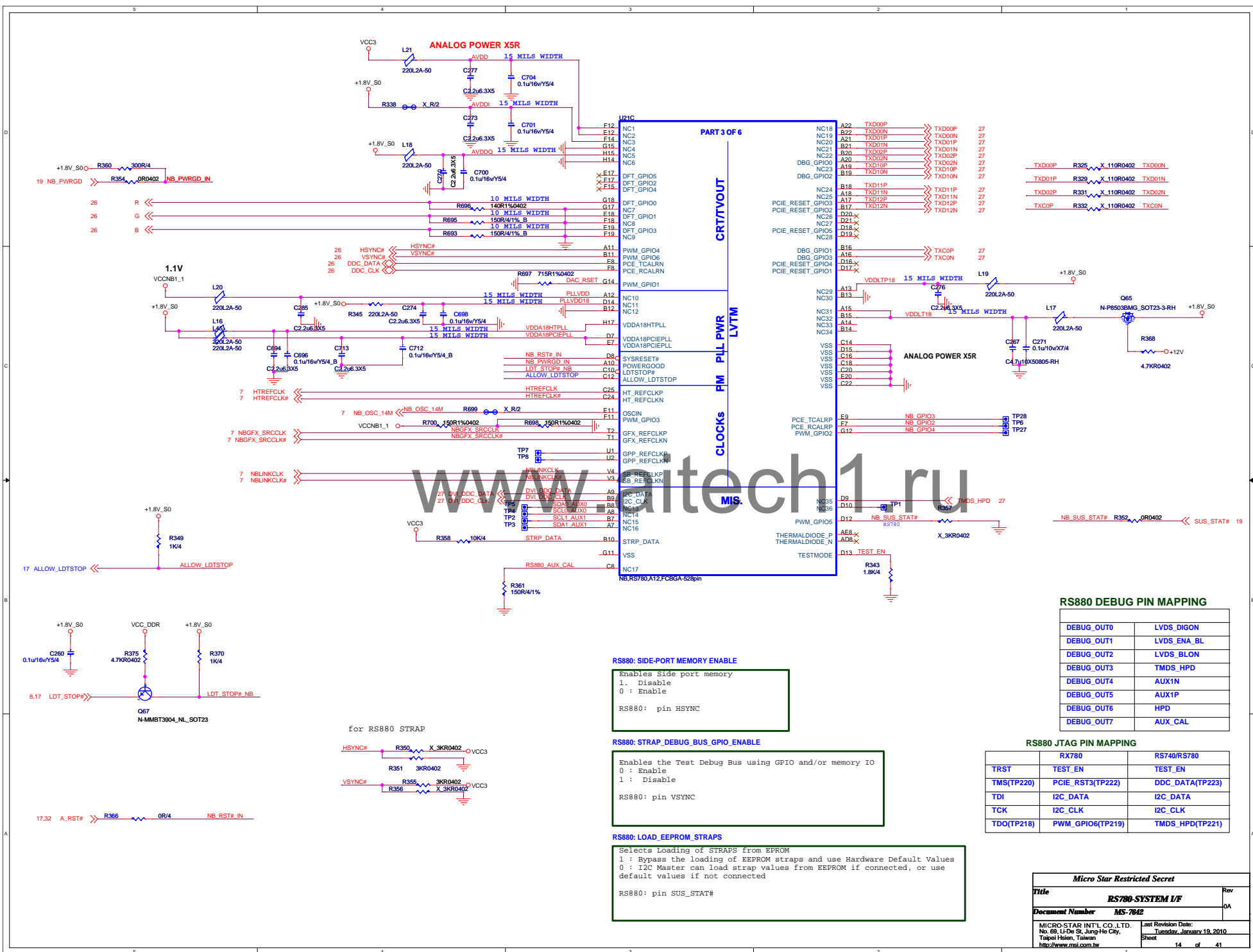
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Title	Intersil 6329CR 3 Phase	Rev
Document Number	MS-7642	0A
MICRO STAR INT'L CO. LTD. No. 69, Li-De St., Jung-Huei City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, January 19, 2010 Sheet 6 of 41

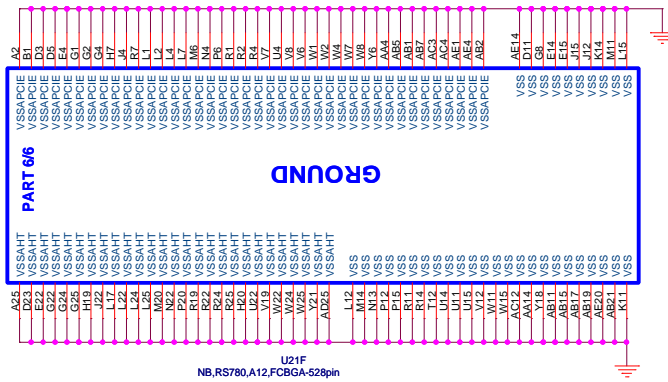






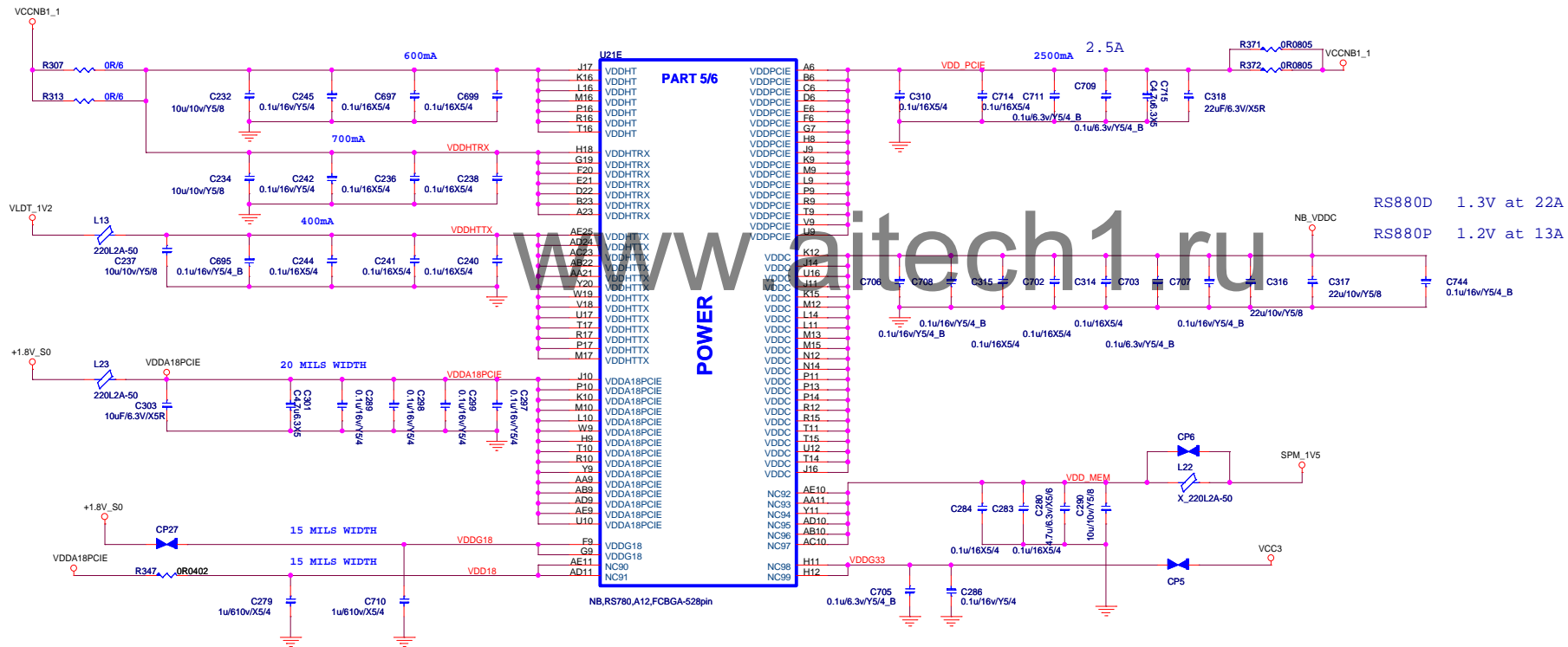


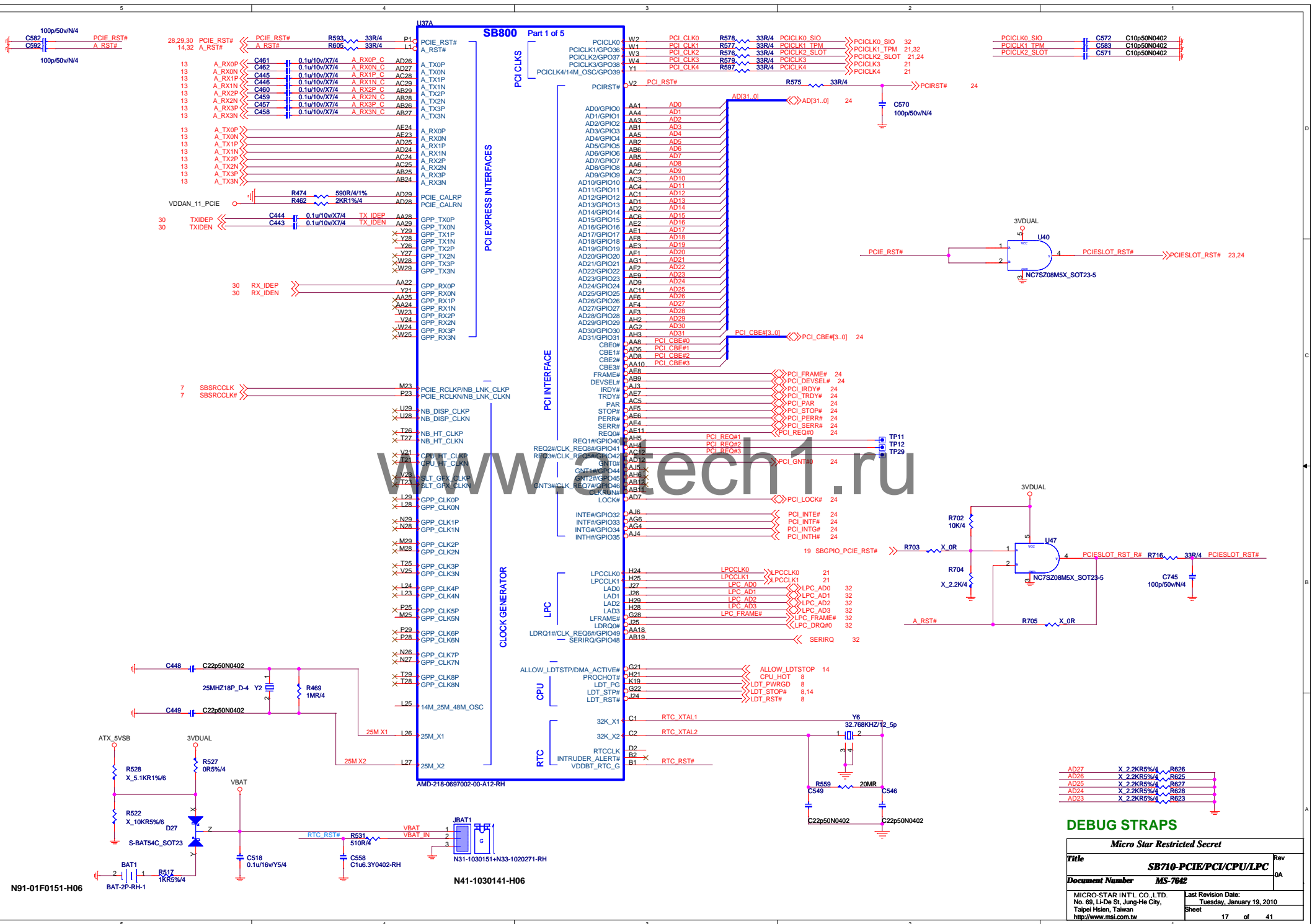


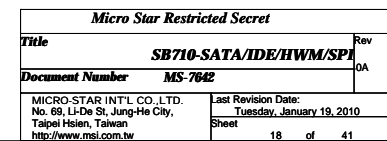


RS880D POWER TABLE

PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDD18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.3V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.5V	VDDLTP18	+1.8V
VDD33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC







PCI_PME# internal pull high 10k to 3V

24,32 PCI_PME# << PCI PME# R566 X 0R5%/4 SB PME#

29,32,34,37 SLP_S3# << SLP_S3#
29,32,34,36 SLP_S5# << SLP_S5#
32 PWRBTN# << PWRBTN#
37 SB_PWRGD << SB_PWRGD
14 SUS_STAT# << SUS_STAT#

32 A20GATE << A20GATE
32 KBRST# << KBRST#
32 LPC_PME# << LPC_PME#

7,37 FP_RST# << FP_RST#
23,24,28,29,32 PE_WAKE# << PE_WAKE#

8 CPU_THRIP# << CPU_THRIP#
14 NB_PWRGD << NB_PWRGD

32 RSMRST# << RSMRST#

22,23 DUALX8_EN# << DUALX8_EN#

37 SPKR << SPKR

15 SPM_RESET# << SPM_RESET#

7 SB_OSC_14M << SB_OSC_14M

17 SBGPIO_PCIE_RST# << SBGPIO_PCIE_RST#

25 USB_OCP#1 << USB_OCP#1

25,29 USB_OCP#0 << USB_OCP#0

31 AZ_BITCLK << AZ_BITCLK

21,31 AZ_SDOUT << AZ_SDOUT

31 AZ_SDIN0 << AZ_SDIN0

31 AZ_SYNC << AZ_SYNC

31 AZ_RST# << AZ_RST#

31 AZ_RST# << AZ_RST#

31 AZ_RST# << AZ_RST#

31 AZ_RST# << AZ_RST#

31 AZ_RST# << AZ_RST#

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31 AZ_RST# << AZ_RST#

31 AZ_RST# << AZ_RST#

U37D

PCI PME# / GEVENT4#

R# / GEVENT22#

SPI_CS# / GBE_STAT1 / GEVENT21#

SLP_S3#

SLP_S5#

PWR_BTN#

PWR_GOOD

SUS_STAT#

TEST0

TEST1

TEST2

TEST3

TEST4

TEST5

TEST6

TEST7

TEST8

TEST9

TEST10

TEST11

TEST12

TEST13

TEST14

TEST15

TEST16

TEST17

TEST18

TEST19

TEST20

TEST21

TEST22

TEST23

TEST24

TEST25

TEST26

TEST27

TEST28

TEST29

TEST30

TEST31

TEST32

USBCLK/14M_25M_48M_OSC

USB_RCOMP

USB_FSDP/GPIO186

USB_FSDN

USB_FSDOP/GPIO185

USB_FSDON

USB_HSD13P

USB_HSD13N

USB_HSD12P

USB_HSD12N

USB_HSD11P

USB_HSD11N

USB_HSD10P

USB_HSD10N

USB_HSD9P

USB_HSD9N

USB_HSD8P

USB_HSD8N

USB_HSD7P

USB_HSD7N

USB_HSD6P

USB_HSD6N

USB_HSD5P

USB_HSD5N

USB_HSD4P

USB_HSD4N

USB_HSD3P

USB_HSD3N

USB_HSD2P

USB_HSD2N

USB_HSD1P

USB_HSD1N

USB_HSD0P

USB_HSD0N

USB_HSD0P

USB_HSD0N

USB_HSD0P

USB_HSD0N

USB_HSD0P

USB_HSD0N

USB_HSD0P

USB_HSD0N

A10

G19 USB_RCOMP R521 11.8K/4/1%

J10

H10

J8

B12

A12

E11

E14

J12

J14

A13

B13

D13

C13

G12

G14

G16

G18

D16

C16

B14

A14

E18

E16

J16

J18

A17

B17

A16

B16

A15

B15

A14

B14

A13

B13

A12

B12

A11

B11

A10

90 Ohm

GPIO200 GPIO199

ROM TYPE: H, H = Reserved
H, L = SPI ROM
L, H = LPC ROM
L, L = FWH ROM

3VDUAL

3VDUAL

R515 X 2.2KR5%/4

R518 X 2.2KR5%/4

GPIO199

GPIO200

R516 2.2KR5%/4

R519 X 2.2KR5%/4

GPIO199

GPIO200

GPIO199

GPIO200

GPIO199

GPIO200

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GPIO199

GPIO200

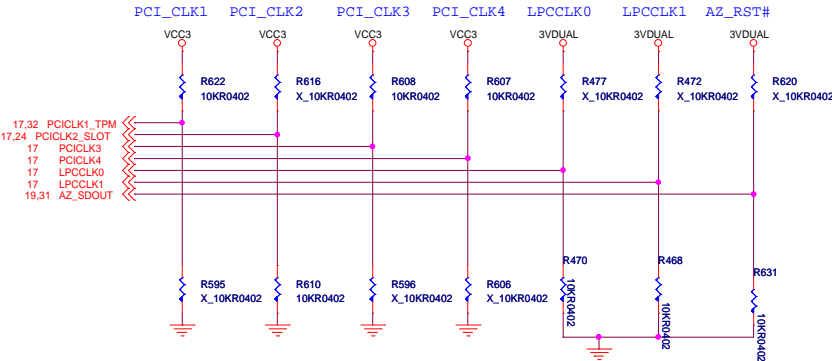
GPIO199

Micro Star Restricted Secret

Title		Rev
SB710-ACPI/GPIO/USB/AUDIO		0A
Document Number		MS-7642
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
No. 69, Li-De St, Jung-Ho City,		Tuesday, January 19, 2010
Taipei Hsien, Taiwan		Sheet
http://www.msi.com.tw		19 of 41

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

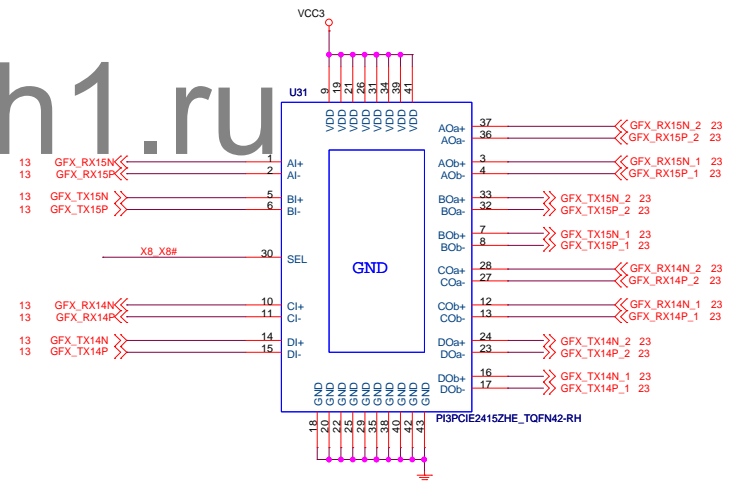
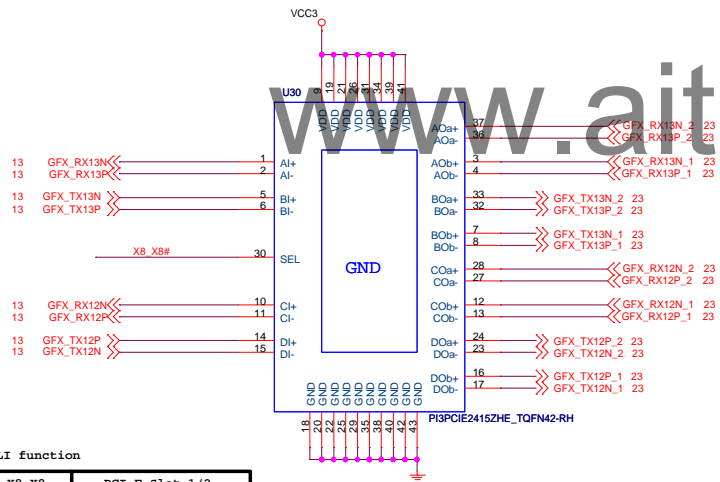
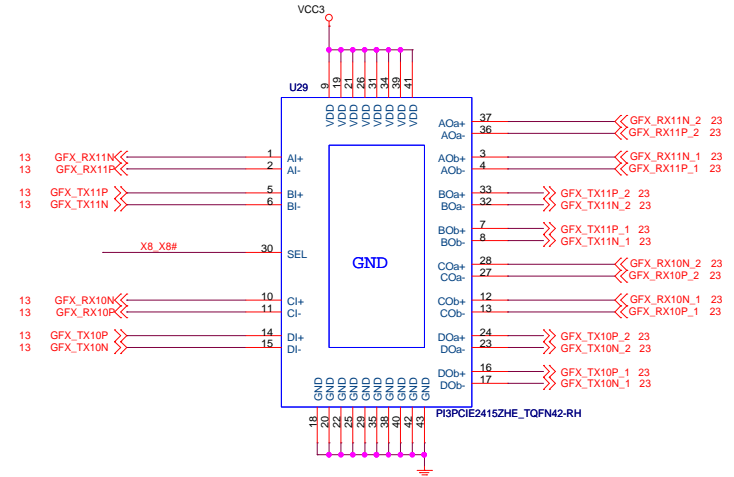
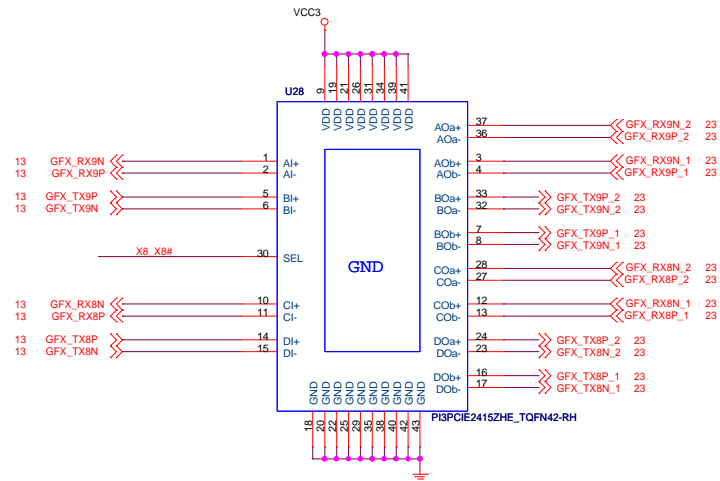


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	
PULL HIGH	CoreSpeedMode Low Power mode	PCIE at GEN2 mode DEFAULT	Watchdog timer Enable	Enable Debug Straps DEFAULT	Reserved DEFAULT	EC ENABLE	Integrated clock mode	
PULL LOW	CoreSpeedMode Performance mode DEFAULT	PCIE at GEN1 mode	Watchdog timer Disable DEFAULT	Disable Debug Straps	Reserved	EC DISABLE DEFAULT	External clock mode DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Digital Switch
SEL pin SLI function

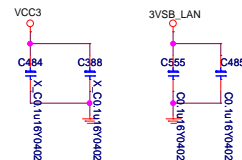
DualX8_En#	Output	X8_X8	PCI-E_Slot 1/2
1	b	1	X16
0	a	0	X8 / X8



PCI EXPRESS x16 Slot

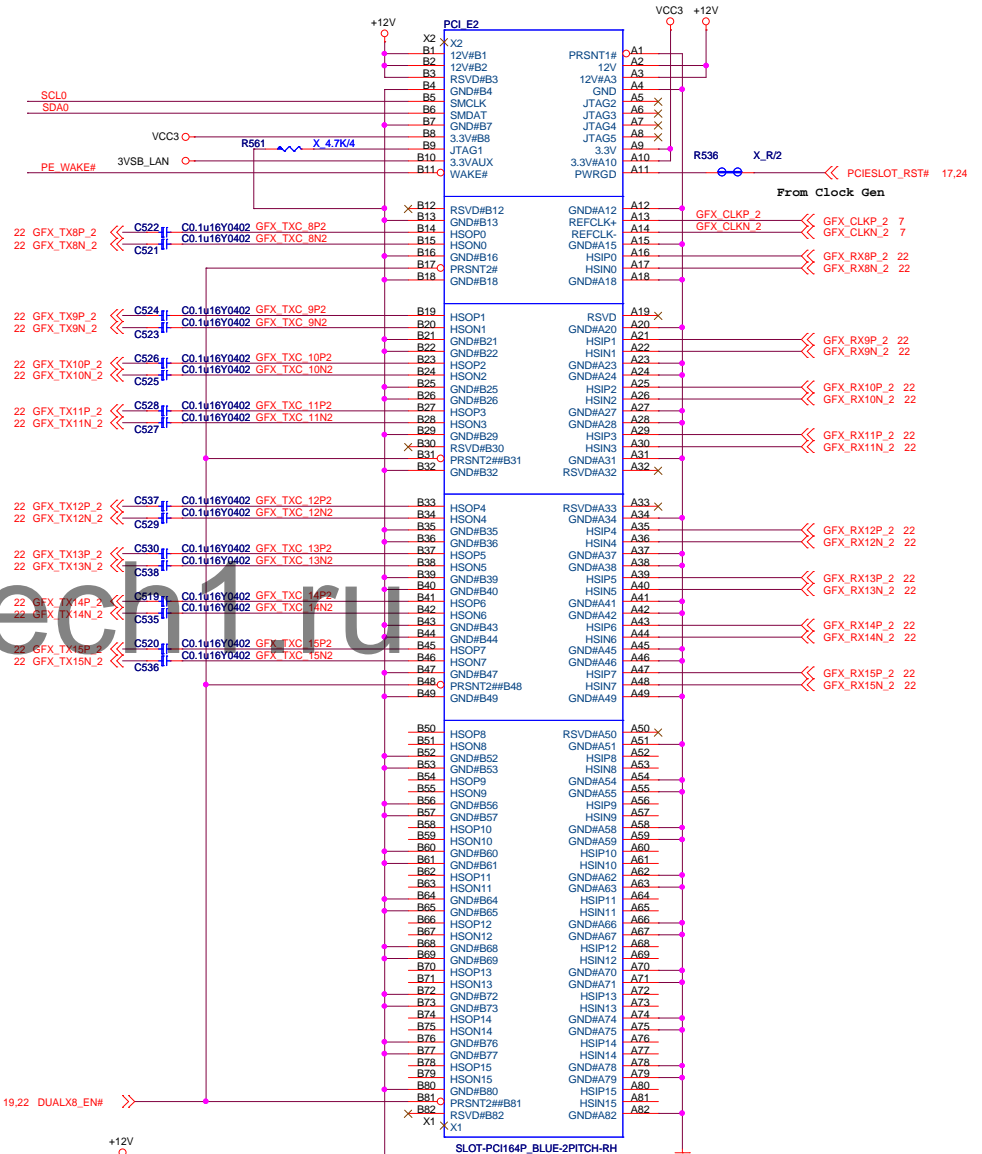


N11-1640401-K06

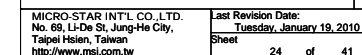


Placement Close To PCIE16_X1

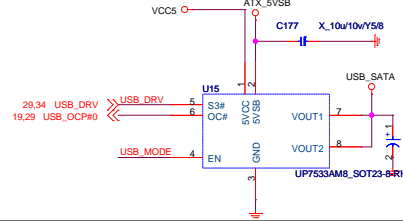
PCI EXPRESS x16 Slot



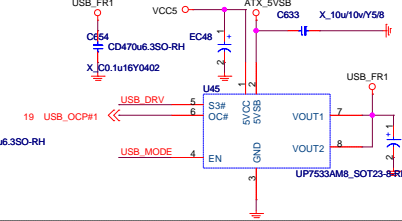
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Title		
PCI EXPRESS X16 & X1 SLOT		
Document Number		
MS-7642		
Last Revision Date:		
Tuesday, January 19, 2010		
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23 of 41		



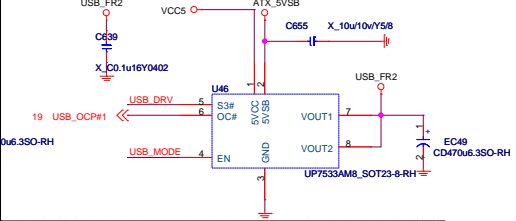
POWER CIRCUIT FOR USB PORT 2,3



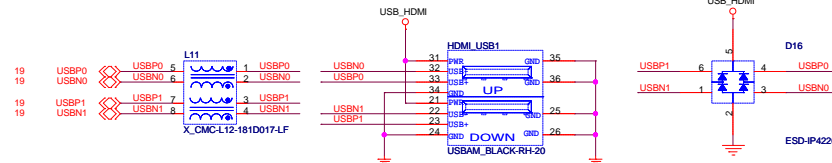
POWER CIRCUIT FOR USB PORT 6,7



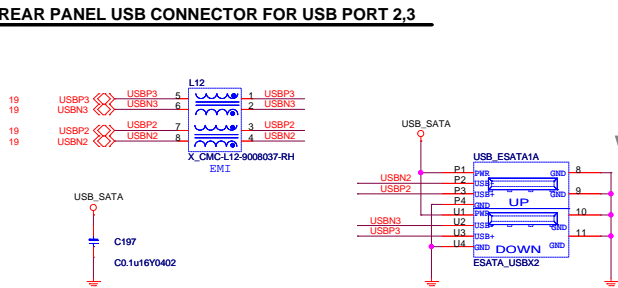
POWER CIRCUIT FOR USB PORT 8,9



REAR PANEL USB CONNECTOR FOR USB PORT 0,1

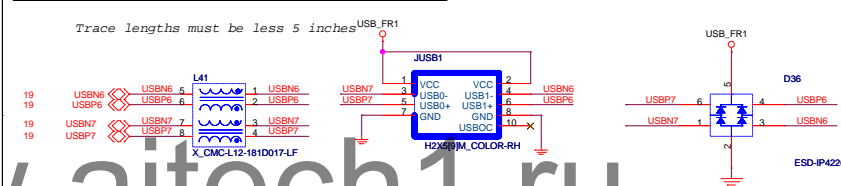


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

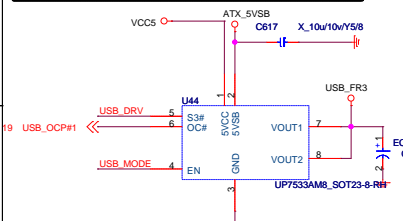


NEAR USB CONNECTOR

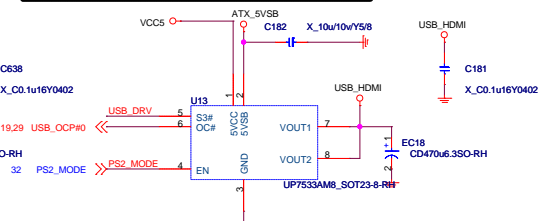
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



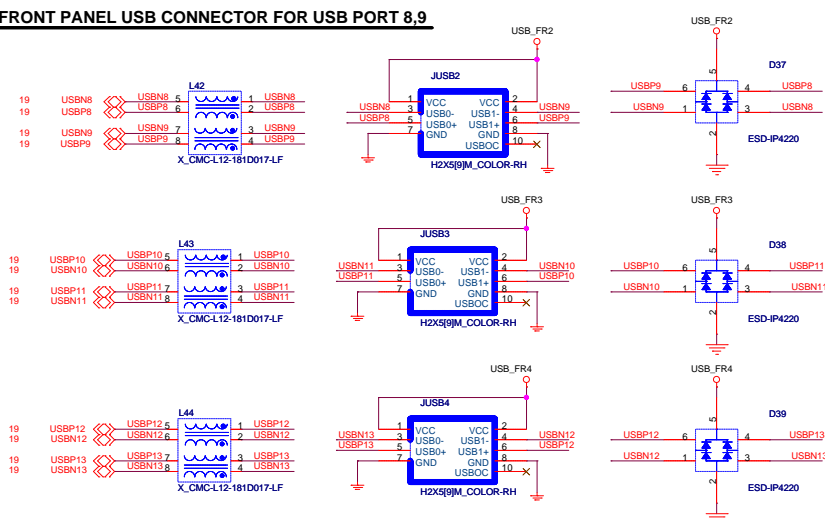
POWER CIRCUIT FOR USB PORT 10,11

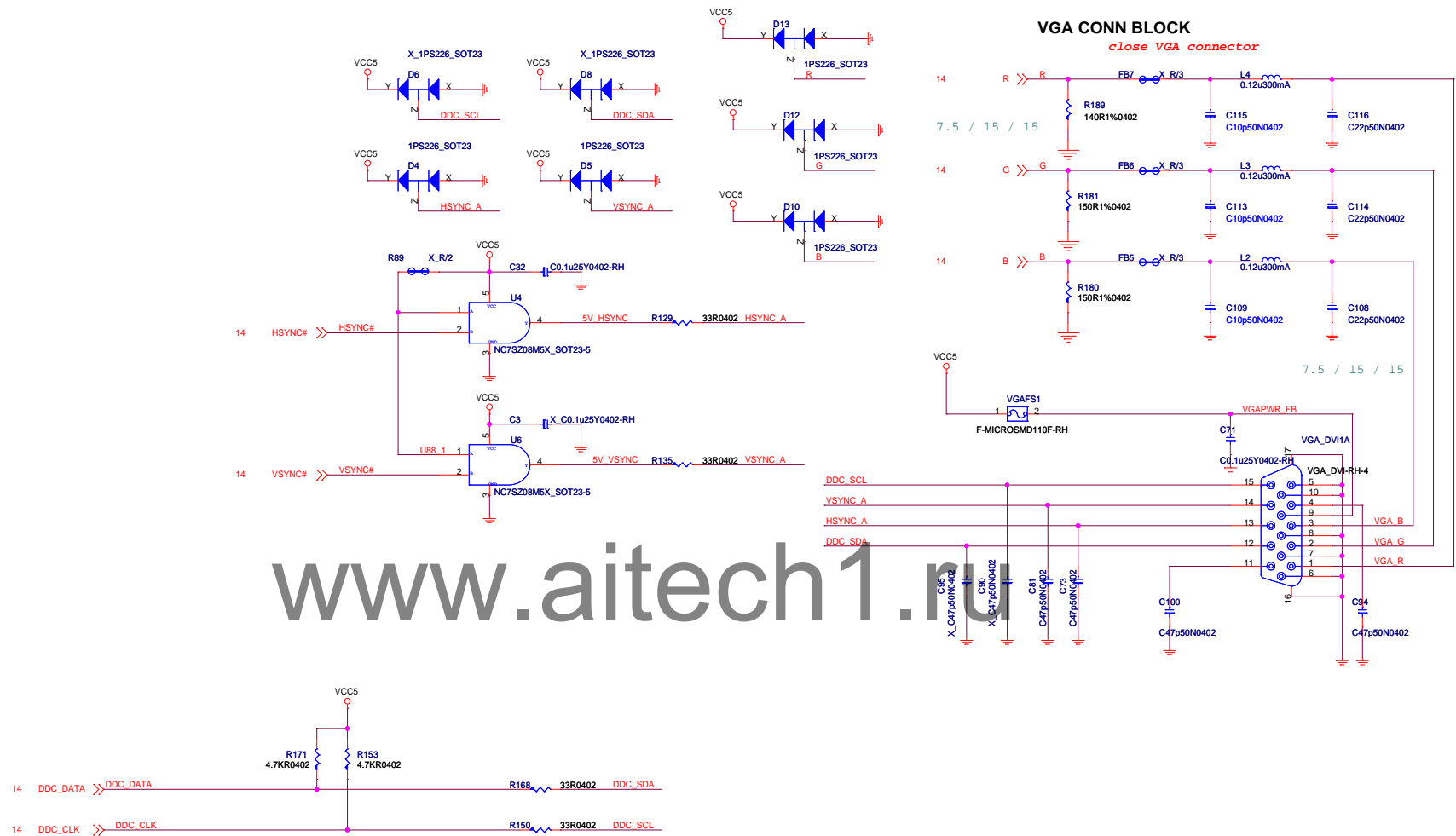


POWER CIRCUIT FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

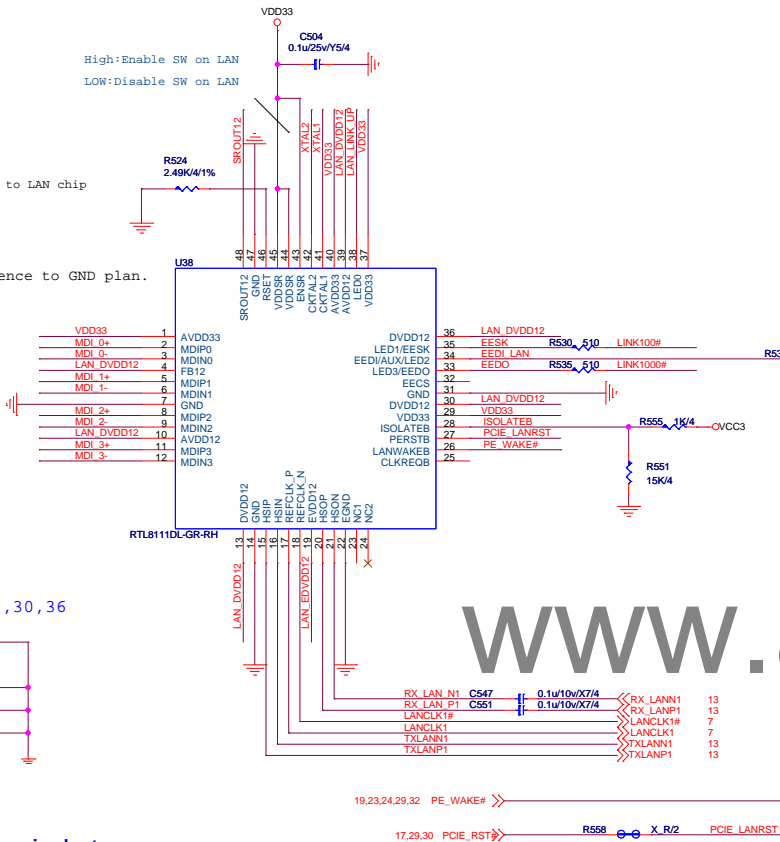




High:Enable SW on LAN
LOW:Disable SW on LAN

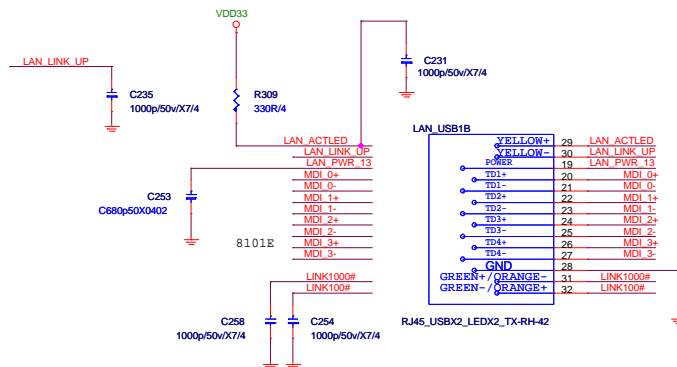
Place R365 close to LAN chip
within 200 mil

MDIx+/- Reference to GND plan.



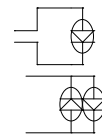
Power domain chart

	RTL8111DL	
AVDD33	3.3V	
VDDSR	3.3V	
VDD33	3.3V	
EVDD12	1.2V	
DVDD12	1.2V	
AVDD12	1.2V	



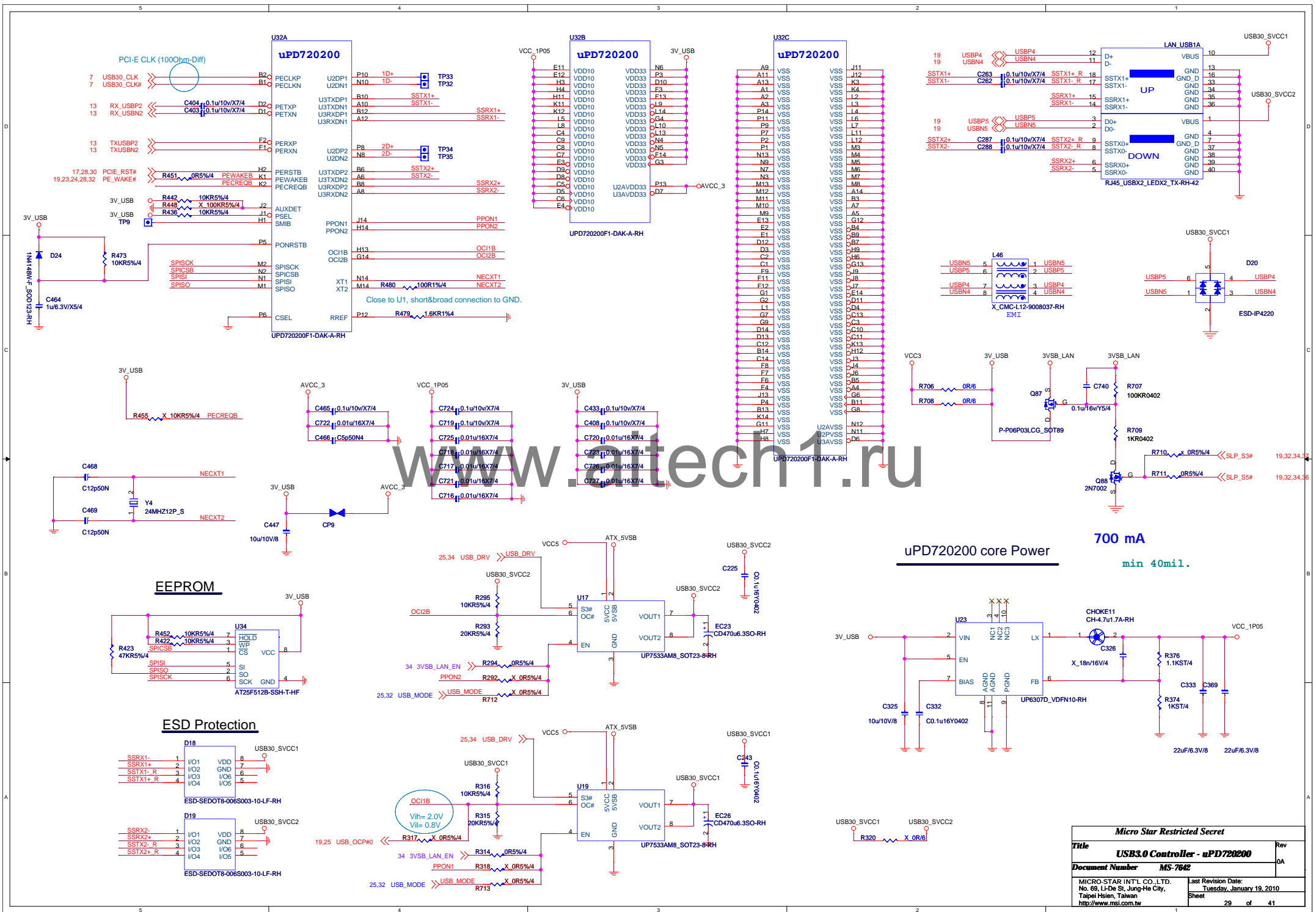
Power consumption			
	1G	100M	
3.3V	103mA	TBD	
1.5V	367mA	TBD	
1.8V	198mA	TBD	

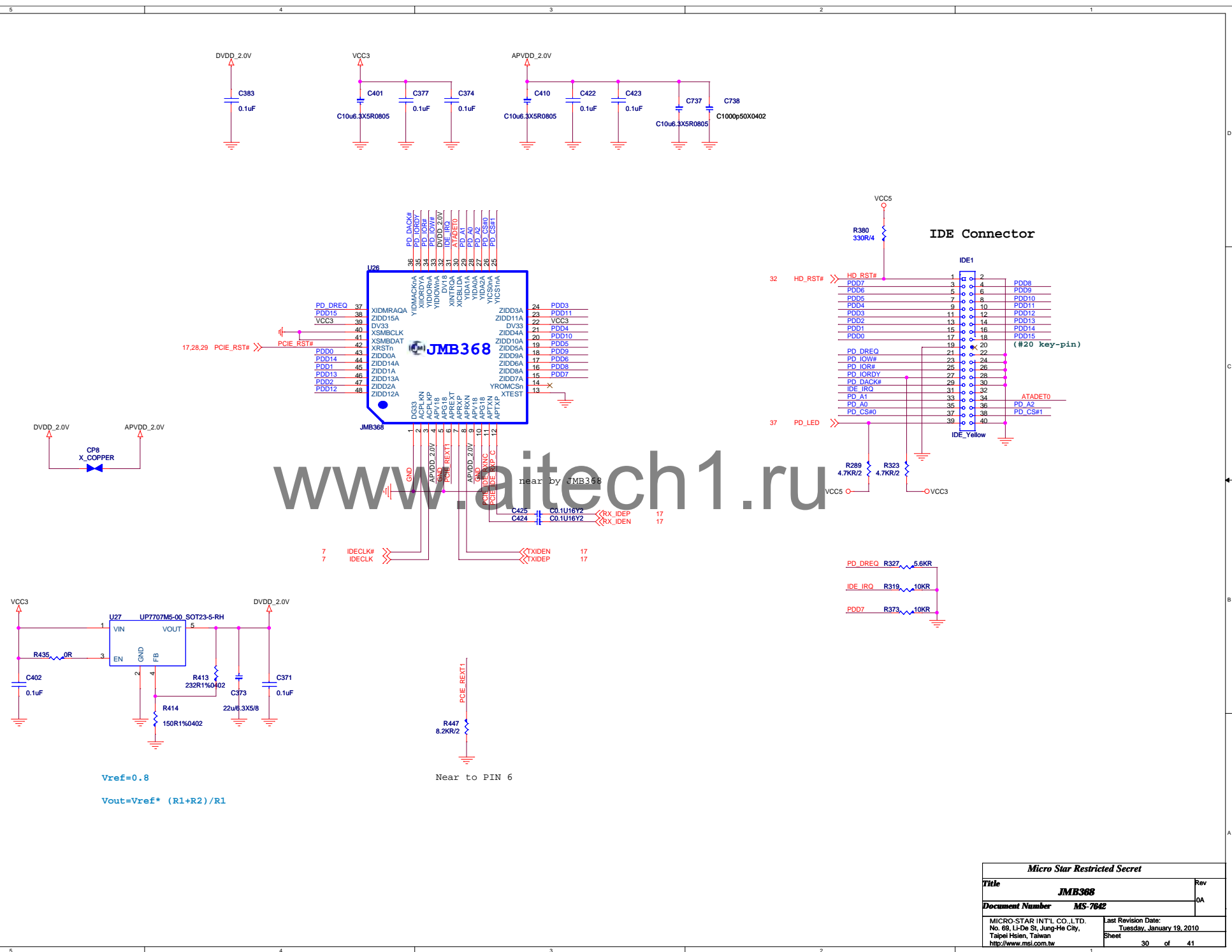
N58-16P0031-F02

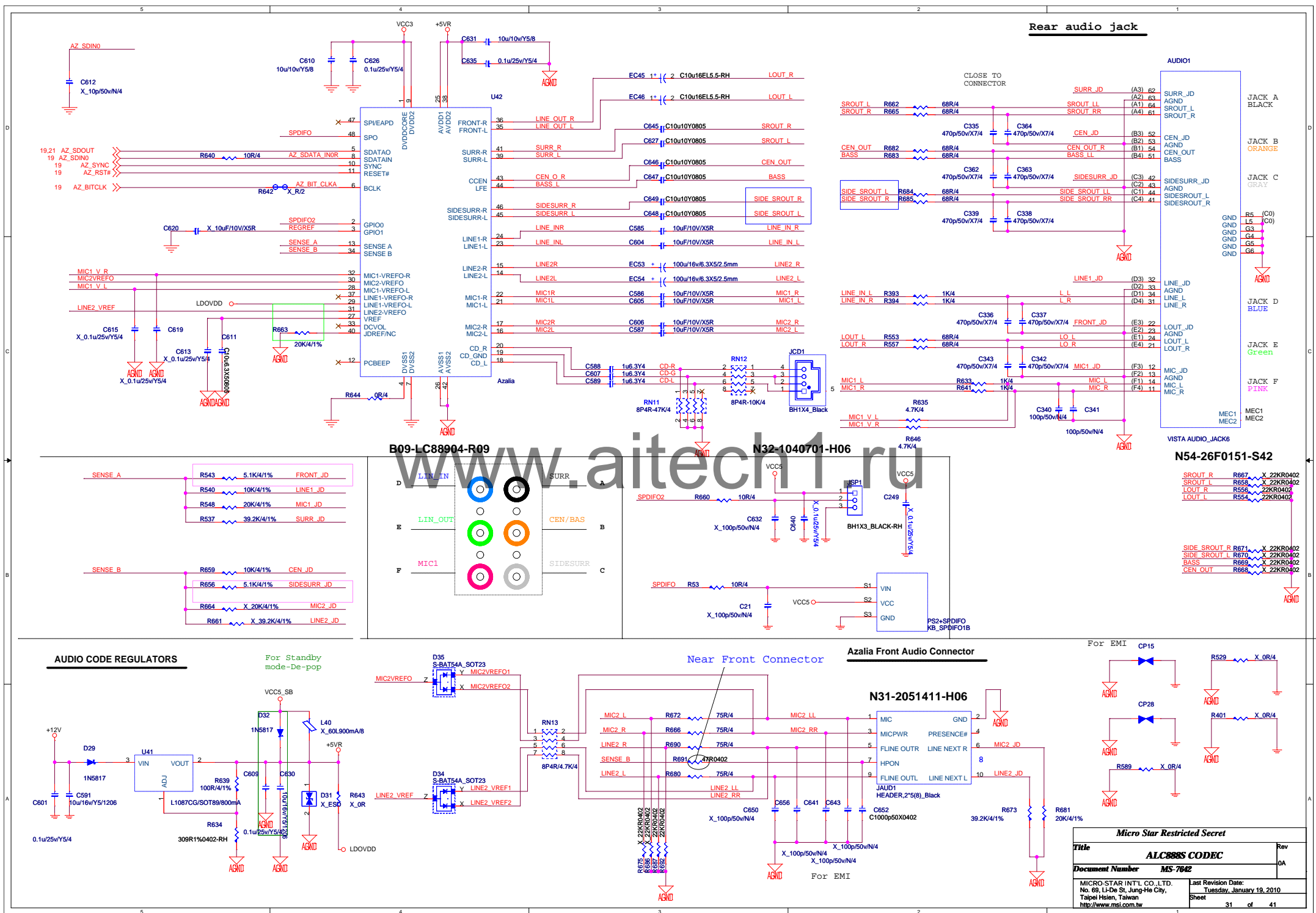


	Giga-Lan	10/100-Lan
	N58-22F0081-S42	N58-22F0061-S42 N58-22F0061-F02
Link	Yellow	Link Yellow
Active	Blinking	Active Blinking
1000	Orange	100 Green
100	Green	10 None
10	None	
19		19
20	Yellow	20 Yellow
21	Orange	21
22	Green	22 Green

Micro Star Restricted Secret			
Title			Rev
LAN - Realtek 8111DL			0A
Document Number			MS-7042
MICRO-STAR INT'L CO., LTD.			Last Revision Date:
No. 69, Li-De St. Jung-Ho City,			Tuesday, January 19, 2010
Taipei Hsien, Taiwan			Sheet
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D41
S-SM5817A

VCC5 ○ A C LPT VC

STB# R674 2.7K0402

S_PD3 1 2

S_PD2 3 4

S_SLIN# 5 6

INIT# 7 8

S_PD7 1 2

S_PD6 3 4

S_PD5 5 6

S_PD4 7 8

RN9 8P4R-2.7K0402

SLCT RN10 8P4R-2.7K0402

PE 1 2

BUSY 3 4

ACK# 5 6

S_PD1 7 8

ERR# 3 4

S_PD0 5 6

AFD# 7 8

RN7 8P4R-2.7K0402

SLCT 32

PE 32

BUSY 32

ACK# 32

S_SLIN# 32

INIT# 32

ERR# 32

AFD# 32

STB# 32

S_PD0 32

S_PD1 32

S_PD2 32

S_PD3 32

S_PD4 32

S_PD5 32

S_PD6 32

S_PD7 32

SLCT 32

PE 32

BUSY 32

ACK# 32

S_SLIN# 32

INIT# 32

ERR# 32

AFD# 32

STB# 32

S_PD0 32

S_PD1 32

S_PD2 32

S_PD3 32

S_PD4 32

S_PD5 32

S_PD6 32

S_PD7 32

Figure 10 shows the pin connections for the BH2X13-BLACK-RH. The diagram is divided into two main sections, each showing a pin header with its connections to various components.

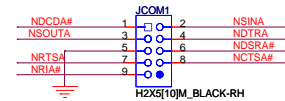
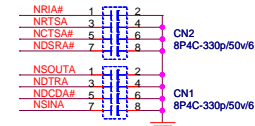
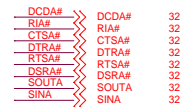
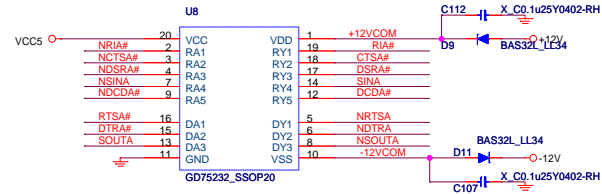
Top Section:

- Pin Header:** STB#, S_PD0, S_PD1, S_PD2, S_PD3, S_PD4, S_PD5, S_PD6, S_PD7, ACK#, BUSY, FE, S_LCT.
- Connections:**
 - STB# is connected to pin 1 of JLP1.
 - S_PD0 is connected to pin 2 of JLP1.
 - S_PD1 is connected to pin 3 of JLP1.
 - S_PD2 is connected to pin 4 of JLP1.
 - S_PD3 is connected to pin 5 of JLP1.
 - S_PD4 is connected to pin 6 of JLP1.
 - S_PD5 is connected to pin 7 of JLP1.
 - S_PD6 is connected to pin 8 of JLP1.
 - S_PD7 is connected to pin 9 of JLP1.
 - ACK# is connected to pin 10 of JLP1.
 - BUSY is connected to pin 11 of JLP1.
 - FE is connected to pin 12 of JLP1.
 - S_LCT is connected to pin 13 of JLP1.

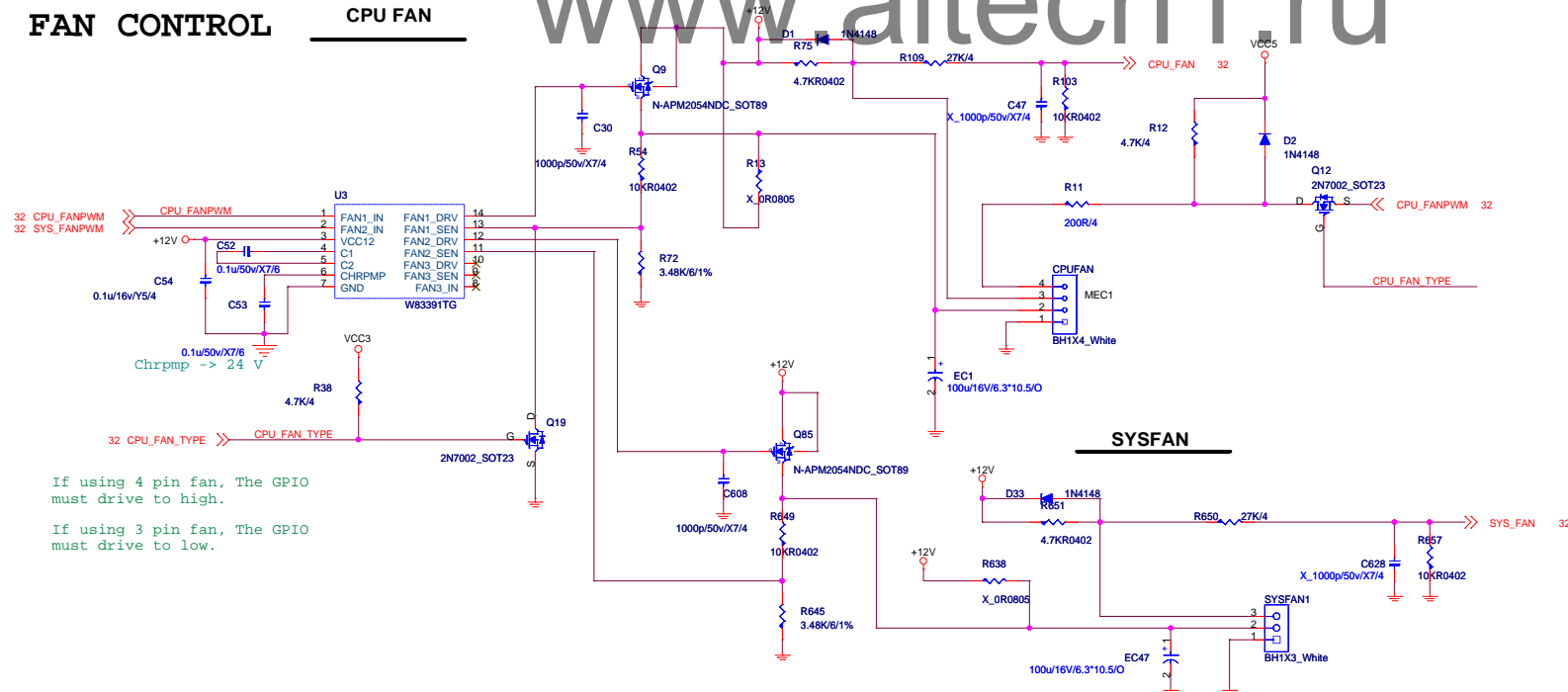
Bottom Section:

- Pin Header:** S_PD3, S_PD2, INIT#, S_PD7, S_PD6, S_PD5, S_LCT, BUSY.
- Connections:**
 - S_PD3 is connected to pin 1 of CN4.
 - S_PD2 is connected to pin 2 of CN4.
 - INIT# is connected to pin 3 of CN4.
 - S_PD7 is connected to pin 4 of CN4.
 - S_PD6 is connected to pin 5 of CN4.
 - S_PD5 is connected to pin 6 of CN4.
 - S_LCT is connected to pin 7 of CN4.
 - BUSY is connected to pin 8 of CN4.

The diagram also shows connections to AFD#, ERR#, INIT#, S_SLIN#, and various CN4, CN5, CN6, and CN3 connectors.

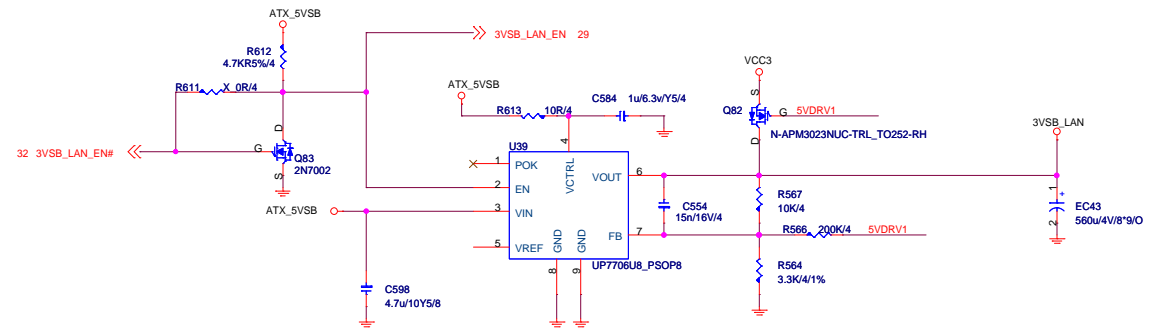
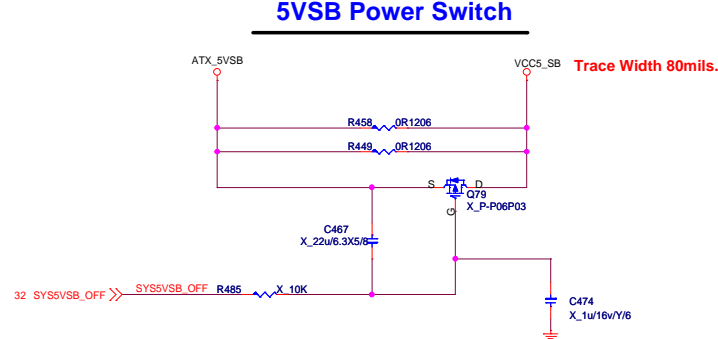


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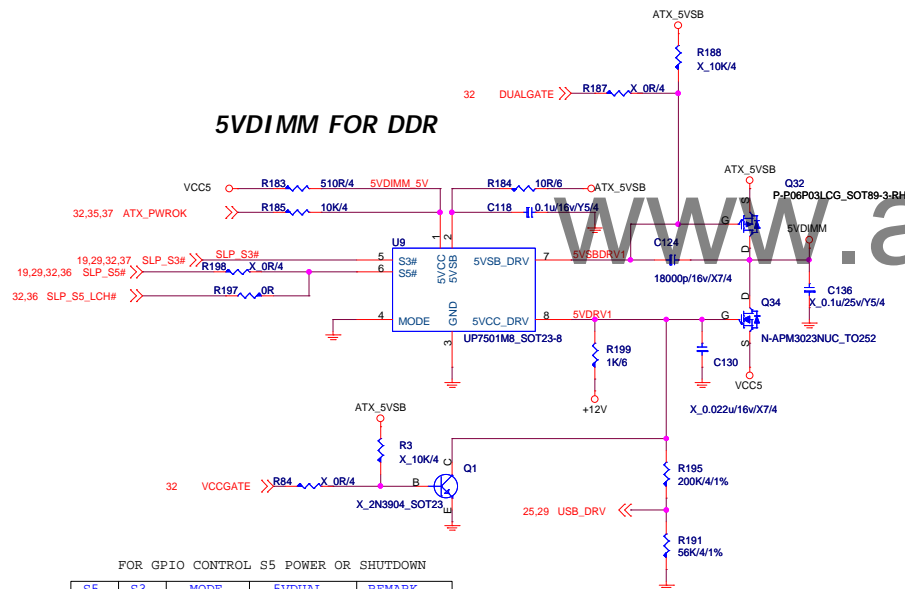


Deep Mode WOL LAN Power CTRL Circuit

5VSB Power Switch

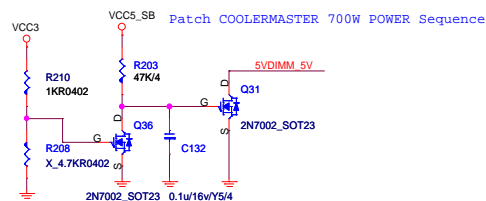


5VDIMM FOR DDR



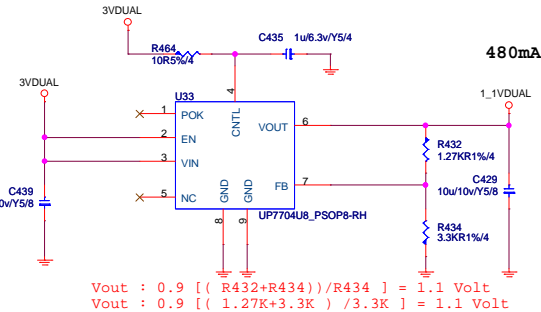
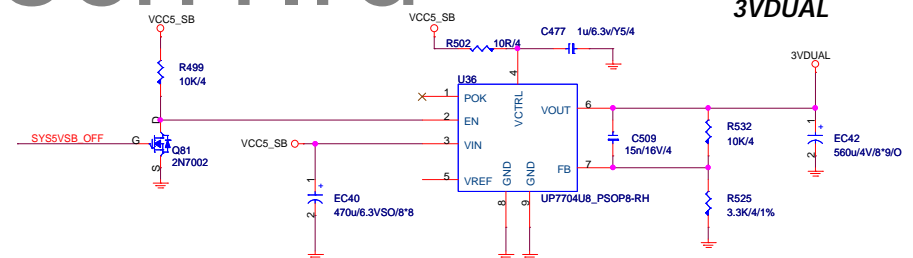
FOR GPIO CONTROL S5 POWER OR SHUTDOWN

S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5



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3VDUAL



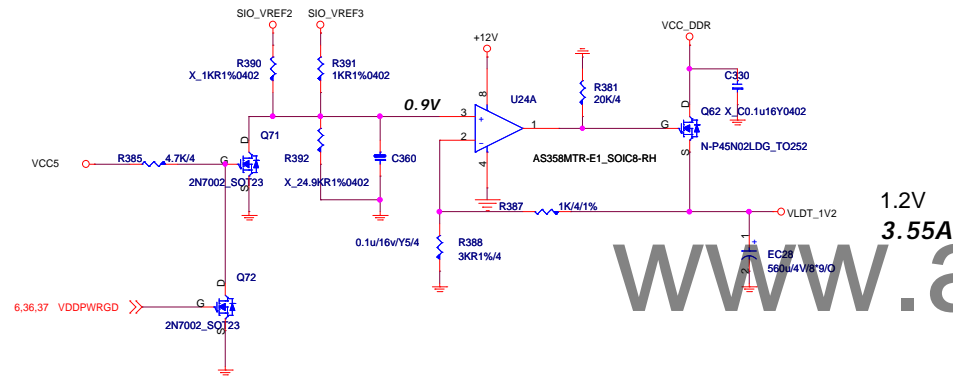
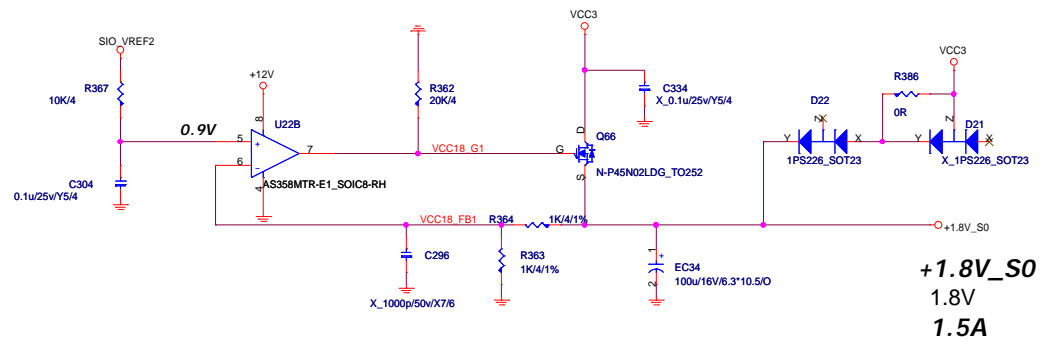
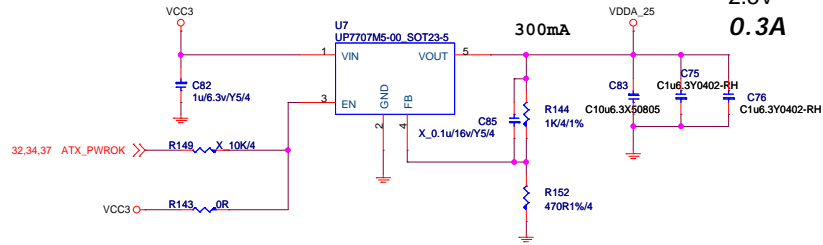
1P1V_SB_DUAL for SB, 480mA S0 - S5

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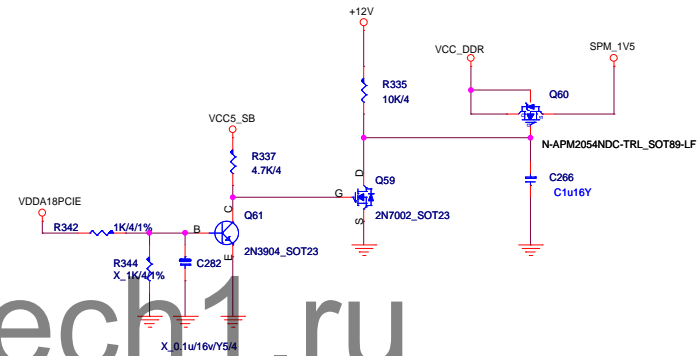
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Document Number	MS-7462	Last Revision Date:	Tuesday, January 19, 2010
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VDDA_25

2.5V
0.3A

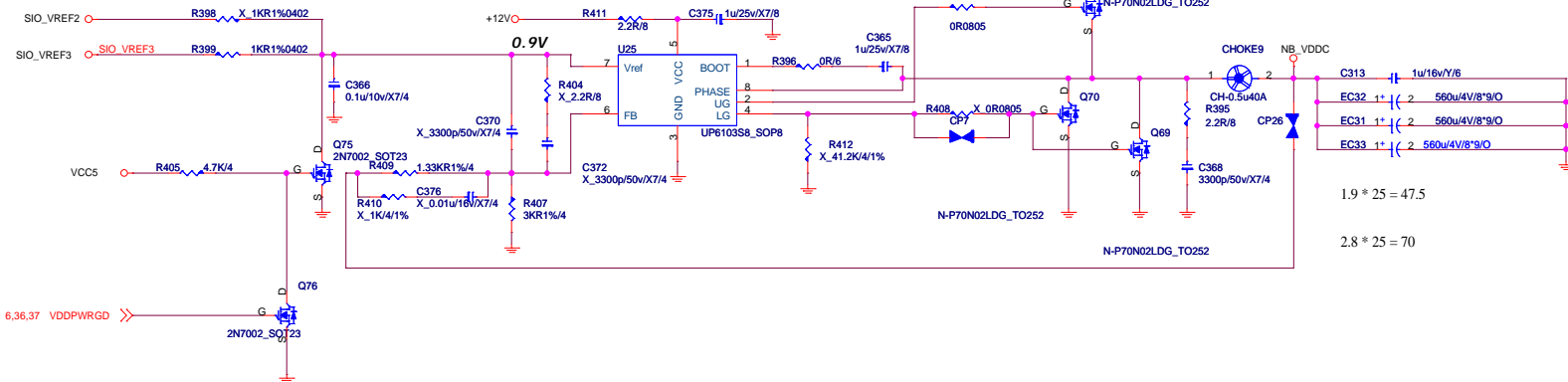


1.2V
3.55A



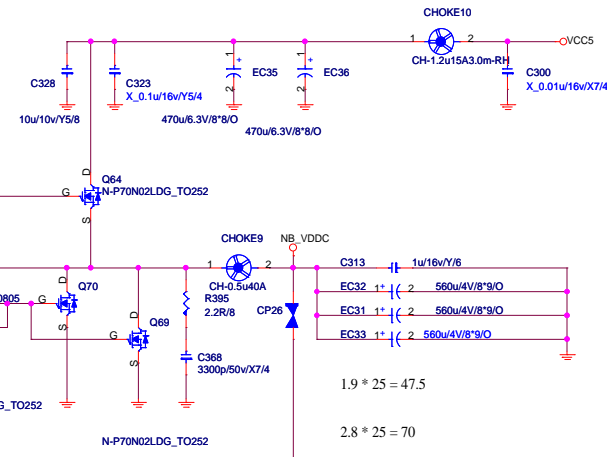
+1.8V_S0
1.8V
1.5A

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NB_VDDC

1.3V 25.8A



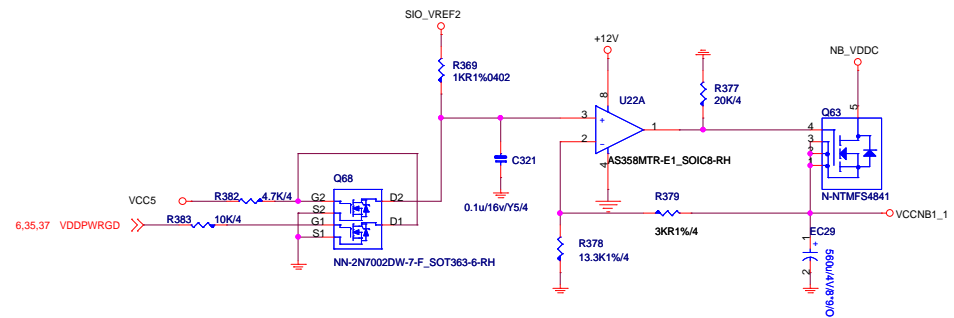
1.9 * 25 = 47.5

2.8 * 25 = 70

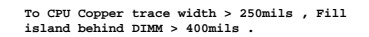
Micro Star Restricted Secret

Title		UPI ACPI	Rev
Document Number		MS-7642	0A
MICRO-STAR INT'L CO., LTD. No. 69, L-Hsueh St., Jung-Hsi City, Taipei Hsien, Taiwan		Last Revision Date: Tuesday, January 19, 2010	
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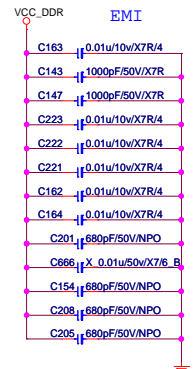
VCCNB1_1 **3.8A**



VTT_DDR 1.5A



OSC CAP:C71-4710621-N07

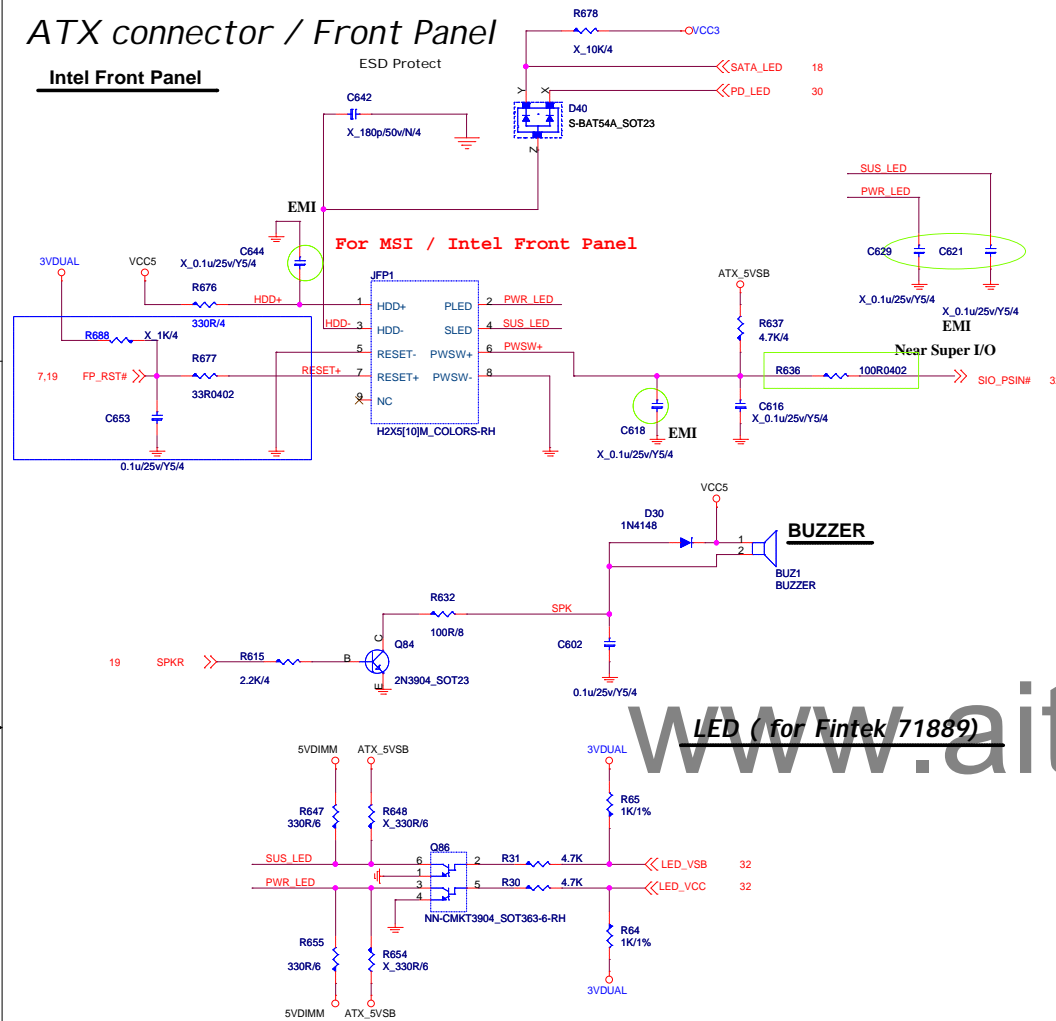


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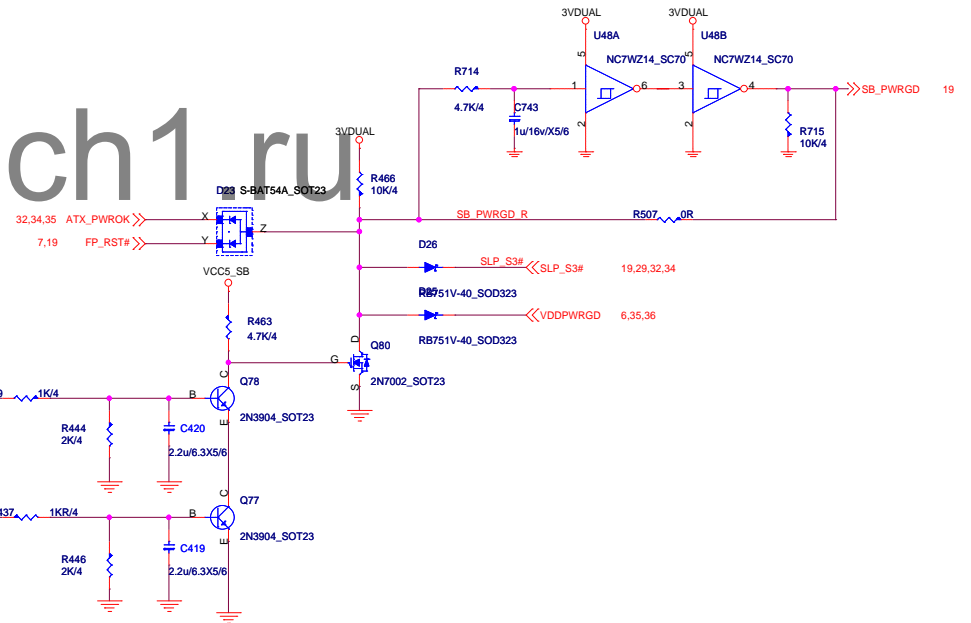
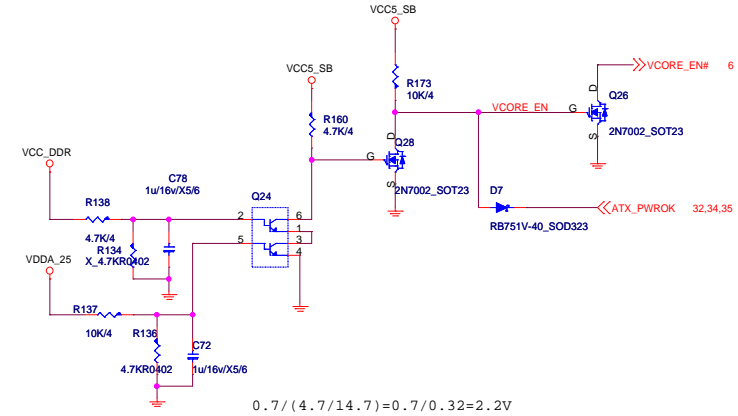
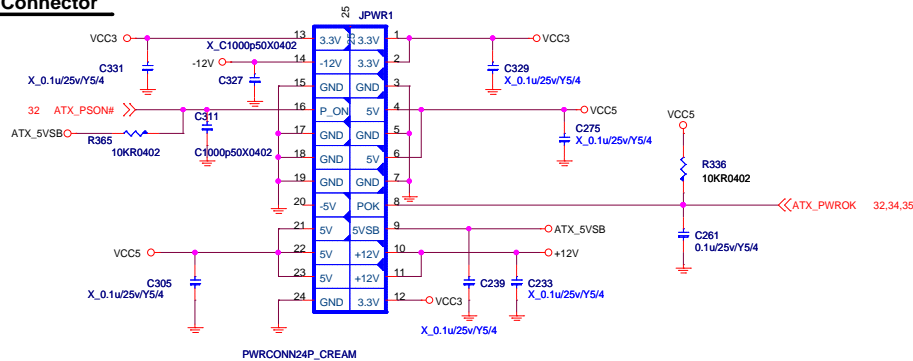
Last Revision Date:	
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ATX connector / Front Panel

Intel Front Panel

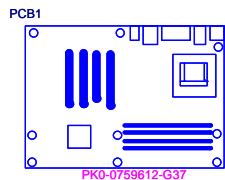


ATX Connector



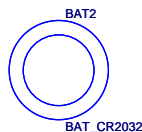
Micro Star Restricted Secret		
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Document Number	MS-7642	0A
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Last Revision Date: Tuesday, January 19, 2010		Sheet
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PCB

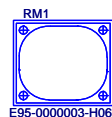


PCB : 1080

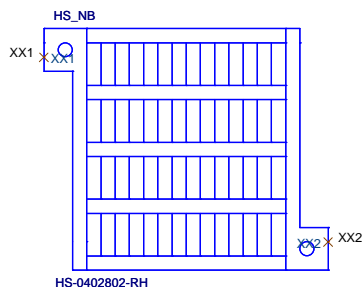
BATTERY



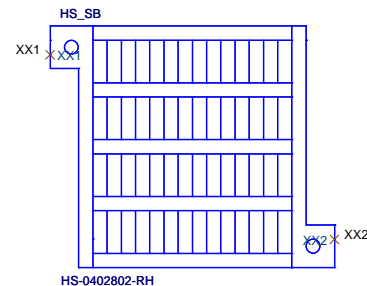
CPU RM



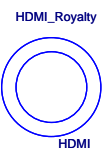
NB HEAT-SINK



SB HEAT-SINK



HDMI



MK1

G51-M1SP540

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Document Number	MS-7642	
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Title	PWROK MAP	Rev
Document Number	MS-7642	0A
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Title	RESET MAP	Rev
Document Number	MS-7842	0A
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Document Number	MS-7642	
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